Digital Electronics

1. Which of the following statements are true ?

I. A circuit that adds two bits, producing a sum bit and a carry bit is called half adder.

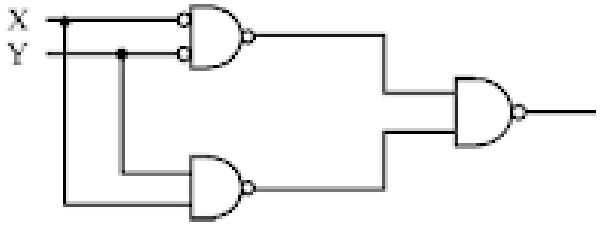
II. A circuit that adds two bits, producing a sum bit and a carry bit is called full adder.

III. A circuit that adds two bits and a carry bit producing a sum bit and a carry bit is called full adder.

IV. A device that accepts the value of a Boolean variable as input and produces its complement is called an inverter.

(A) I & II (B) II & III
(C) I, II, III (D) I, III & IV
Answer: D
(UGCNET-Dec2013-II-40)

2. The output of the following combinational circuit



is :
(A) X . Y (B) X + Y
(C) X □ Y (D) X □ Y
Answer: D
(UGCNET-AUG2016-III-6)

3. A ripple counter is a (n):
(A) Synchronous Counter (B) Asynchronous counter
(C) Parallel counter (D) None of the above
Answer: B
(UGCNET-AUG2016-III-1)

4. Which of the following 2 input Boolean logic functions is linearly inseparable?
(a) AND (b) OR
(c) NOR (d) XOR
(e) NOT XOR

(A) (a) and (b) (B) (b) and (c)
(C) (c), (d) and (e) (D) (d) and (e)
Answer: D
(UGCNET-AUG2016-III-65)

5. Which of the following is a sequential circuit?

(A) Multiplexer (B) Decoder

(C) Counter (D) Full adder

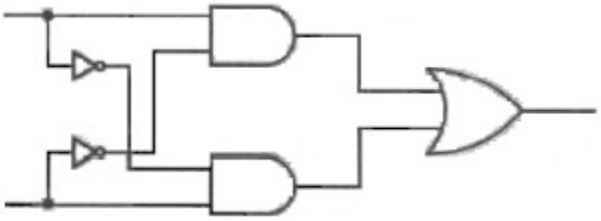
Answer: C

(UGCNET-June2016-III-1)

6. Which of the following flip-flops is free from race condition?
   (A) T flip-flop
   (B) SR flip-flop
   (C) Master-slave JK flip-flop
   (D) None of the above
   Answer: C
   (Q44,p3,J14.)

7. The output of a sequential circuit depends on
   (A) present input only
   (B) past input only
   (C) both present and past input
   (D) past output only
   Answer: C
   (UGCNET-June2014-III-42)

8. What will be the output of the following logic diagram?



   (A) x OR y
   (B) x AND y
   (C) x XOR y
   (D) x XNOR y
   Answer: C
   (UGCNET-Dec2013-III-53)

9. The power dissipation of a flip-flop is 3 mW. The power dissipation of a digital system with 4 flip-flops is given by
   (A) 34 mW
   (B) 43 mW
   (C) 4/3 mW
   (D) 12 mW
   Answer: D
   (UGCNET-Sep2013-III-34)

10. An astable multivibrator using the 555 timer to generate a square wave of 5 KHz with 70% duty cycle will have
    (A) R_A = 40.4 KΩ, R_B = 17.25 KΩ, C = 2000 pF
    (B) R_A = 17.25 KΩ, R_B = 40.4 KΩ, C = 2000 pF
    (C) R_A = 40.4 KΩ, R_B = 17.25 KΩ, C = 5000 pF
    (D) R_A = 17.25 KΩ, R_B = 40.4 KΩ, C = 5000 pF
    Answer: Marks given to all
    (UGCNET-Sep2013-III-35)

11. A binary ripple counter is required to count up to 16383. How many flip-flops are required?
    (A) 16382
    (B) 8191
    (C) 512
    (D) 14
    Answer: D
    (UGCNET-Sep2013-III-36)

12. Which logic family dissipates the minimum power?
    (A) DTL
    (B) TTL
    (C) ECL
    (D) CMOS
    Answer: D
    (UGCNET-Sep2013-III-30)

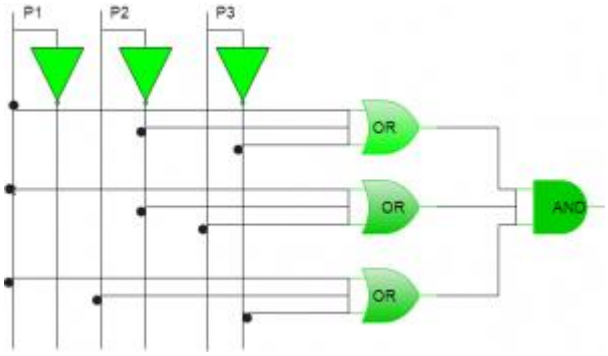
13. Which of the following electronic component is not found in IC's?
    (A) Diode
    (B) Resistor
    (C) Transistor
    (D) Inductor
    Answer: D
    (UGCNET-Sep2013-III-31)

14. The Boolean function with the Karnaugh map

CD \ AB	00	01	11	10
00	0	1	1	0
01	0	1	1	1
11	1	1	1	1
10	0	1	1	0

is :
(1) (A + C).D + B
(2) (A + B).C + D
(3) (A + D).C + B
(4) (A + C).B + D
Answer: 1
(UGC net paper2_nov2017 No 6)

15. The output of the following combinational circuit is F.



The value of F is :
(1) $P_1+P_2'P_3$
(2) $P_1+P_2'P_3'$
(3) $P_1+P_2P_3'$
(4) $P_1'+P_2P_3$
Answer: 2
(UGC-NET CS 2017 Dec 2 | Question 50)

16. The Karnaugh map for a Boolean function is given as

AB \ CD	C`D`	C`D	CD	CD`
A`B`	0	0	0	0
A`B	0	0	1	0
AB	1	1	1	1
AB`	0	1	1	1

The simplified Boolean equation for the above Karnaugh Map is

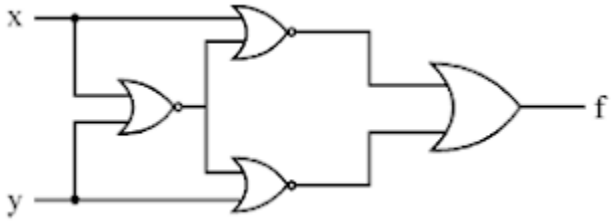
(A) AB + CD + AB' + AD (B) AB + AC + AD + BCD

(C) AB + AD + BC + ACD (D) AB + AC + BC + BCD

Answer: B

(UGC-NET | UGC NET CS 2016 Aug – II | Question 8)

17. Which of the following logic operations is performed by the following given combinational circuit ?



(A) EXCLUSIVE-OR (B) EXCLUSIVE-NOR

(C) NAND (D) NOR

Answer: A

(UGCNET-AUG2016-II-9)

18. Match the following:

List – I	**List – II**
a. Controlled Inverter	i. a circuit that can add 3 bits
b. Full adder	ii. a circuit that can add two binary numbers
c. Half adder	iii. a circuit that transmits a binary word or its 1's complement
d. Binary adder	iv. a logic circuit that adds 2 bits

Codes :

	a	b	c	d
(A)	iii	ii	iv	i
(B)	ii	iv	i	iii
(C)	iii	iv	i	ii
(D)	iii	i	iv	ii

Answer: D

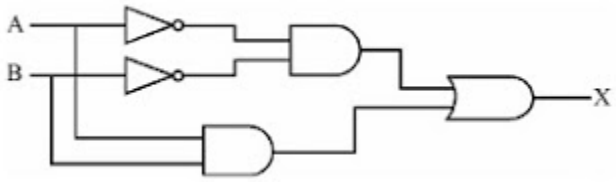
(UGCNET-AUG2016-II-10)

19. In a positive-edge-triggered JK flip-flop, if J and K both are high then the output will be ..... on the rising edge of the clock.
(A) No change (B) Set
(C) Reset (D) Toggle
Answer: D
(UGCNET-June2016-II-10)

20. The BCD adder to add two decimal digits needs minimum of
(A) 6 full adders and 2 half adders
(B) 5 full adders and 3 half adders
(C) 4 full adders and 3 half adders
(D) 5 full adders and 2 half adders
Answer: D
(Paper-2 UGC-NET Computer Science December 2014 No 6)

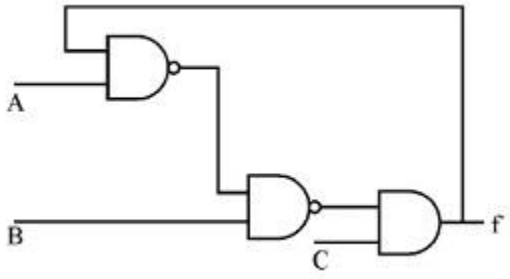
21. Which one of the following set of gates is best suited for 'parity' checking and 'parity' generation?
(A) AND, OR, NOT (B) NAND, NOR
(C) EX-OR, EX-NOR (D) None of the above
Answer: C
(UGCNET-Sep2013-II-23)

22. What type of logic circuit is represented by the figure shown below?



(A) XOR (B) XNOR
(C) XAND (D) XNAND
Answer: B
(UGCNET-Sep2013-II-49)

23. Consider the circuit shown below. In a certain steady state, Y is at logical 'l'. What are possible values of A, B, C ?



(A) A = 0, B = 0, C = 1 (B) A = 0, B = C = 1

(C) A = 1, B = C = 0 (D) A = B = 1, C = 1
Answer: A or D
(UGCNET-Dec2012-II-1)

24. Match the following IC families with their basic circuits :
a. TTL 1. NAND
b. ECL 2. NOR
c. CMOS 3. Inverter
Code :

a	b	c

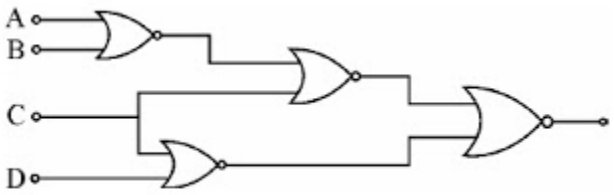
(A) 1 2 3
(B) 3 2 1
(C) 2 3 1
(D) 2 1 3
Answer: A
(UGCNET-Dec2012-II-38)

25. A latch is constructed using two cross-coupled
(A) AND and OR gates (B) AND gates
(C) NAND and NOR gates (D) NAND gates
Answer: D
(UGCNET-June2011-II-8)

26. A multiplexer is a logic circuit that
(A) accepts one input and gives several output
(B) accepts many inputs and gives many output
(C) accepts many inputs and gives one output
(D) accepts one input and gives one output
Answer: C
(UGC NET Paper II - June 2011 No 37)

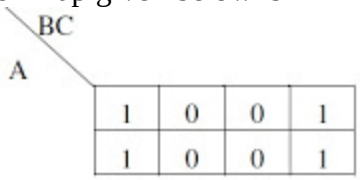
27. An astable multivibrator has
(A) one stable state
(B) two stable states
(C) no stable states
(D) none of these
Answer: C
(UGCNET-Dec2010-II-8)

28. The logic expression for the output of the circuit shown in the figure is



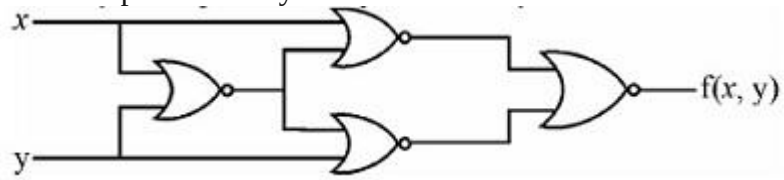
(A) A'C'+B'C'+CD
(B) AC'+BC'+C'D
(C) ABC+C'D'
(D) A'B'+B'C'+C'D'
Answer: C
(UGCNET-june2007- No 9)

29. The function represented by the kmap given below is



(A) A.B
(B) AB+BC+CA
(C) (B□C)'
(D) A.B.C
Answer: C
(UGC net 1998-PP2. No 7)

30. Identify the logic function performed by the circuit shown



(A) exclusive OR
(B) exclusive NOR
(C) NAND
(D) NOR
Answer: B
(UGC NET JUNE 2005 COMPUTER SCIENCE PAPER 2 No 10)

31. An example of a universal building block is:
(A) EX-OR gate
(B) AND gate
(C) OR gate
(D) NOR gate
Answer: D
(UGCNET-dec2008-ii-5)

32. If 4 input multiplexers drive a 4 input multiplexer, we get a:

(A) 16 input MUX
(B) 8 input MUX
(C) 4 input MUX
(D) 2 input MUX
Answer: A
(UGCNET-dec2008-ii-15)

33. Among the logic families RTL, TTL, ECL and CMOS, the fastest family is:
(A) ECL
(B) CMOS
(C) TTL
(D) RTL
Answer: A
(UGC NET Paper II June 2008 No 7)

34. Amongst the logic families DTL, TTL, ECL and CMOS, the family with the least power dissipation is:
(A) CMOS (B) DTL
(C) TTL (D) ECL
Answer: A

35. A sum of products expression can be implemented with.....logic gates.
(A) AND – OR (B) NAND – OR
(C) AND – NOT (D) OR – AND
Answer: A
(Dec 2006 UGC net computer science paper 2 No 8)

36. The characteristic equation of the D flip-flop is:
(A) $Q_{n+1} = D$ (B) $Q = D$
(C) $Q = 1$ (D) $Q = 0$
Answer: A
(UGCNET-dec2008-ii-14)

37. Which of the following logic has the maximum fan out ?
(A) RTL
(B) ECL
(C) NMOS
(D) CMOS
Answer: D
(UGC net June 2006 Paper - II No 8)

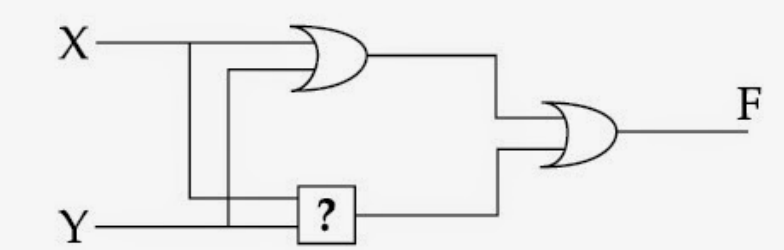
38. Upto how many variables, can the Karnaugh map be used ?
(A) 3
(B) 4
(C) 5

(D) 6
Answer: D
(UGC net June 2006 Paper - II No 10)

39. A half-adder is also known as :
(A) AND Circuit (B) NAND Circuit
(C) NOR Circuit (D) EX-OR Circuit
Answer: D
(UGC NET Paper-2 December 2005 No 7)

40. Consider the following sequence of instructions:
a=a⊕b, b=a⊕b, a=b⊕a. This sequence
(A) retains the value of the a and b
(B) complements the value of a and b
(C) swap a and b
(D) negates values of a and b
Answer: C
(UGC NET PaperII-Dec2005 No 8)

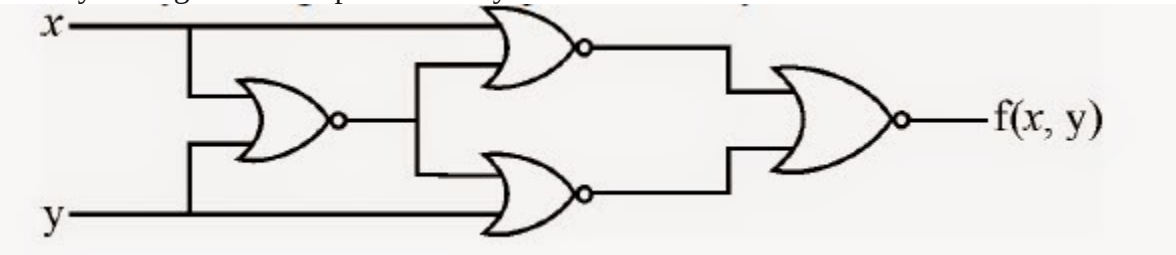
41. Consider the following circuit:



to make it a Tautology the [?] should be:
(A) NAND gate (B) AND gate
(C) OR gate (D) EX-OR gate
Answer: A
(UGC net December 2005 PP2 No 9)

42. When an inverter is placed between both inputs of an S-R flip flop, the resulting flip flop is:
(A) JK flip-flop (B) D flip-flop
(C) T flip-flop (D) None of these
Answer: B
(UGC NET Paper-2 December 2005 No 10)

43. Identify the logic function performed by the circuit shown



(A) Exclusive-OR (B) AND
(C) Exclusive-NOR (D) NOR
Answer: C
(UGC NET JUNE 2005 PAPER 2 No 10)

44. Which of the following logic has the maximum fan out?
(A) RTL (B) ECL
(C) N MOS (D) C MOS
Answer: D
(UGC NET Computer Science Paper-2 June 2005 No 8)

45. Advantage of synchronous sequential circuits over asynchronous ones is
(A) faster operation
(B) ease of avoiding problems due to hazard
(C) lower hardware requirement
(D) better noise immunity
Answer: A

46. What is the transitive voltage for the voltage input of a CMOS operating from 10V supply?
(A) 1V
(B) 2V
(C) 5V
(D) 10 V
Answer: C
(UGCNET-June2010-II-8)

47. The highest noise margin is offered by
(A) BICMOS
(B) TTL
(C) ECL
(D) CMOS
Answer: B
(UGCNET-dec2009-ii-08)

48. Extremely low power dissipation and low cost per gate can be achieved in:
(A) MOS ICs
(B) CMOS ICs
(C) TTL ICs

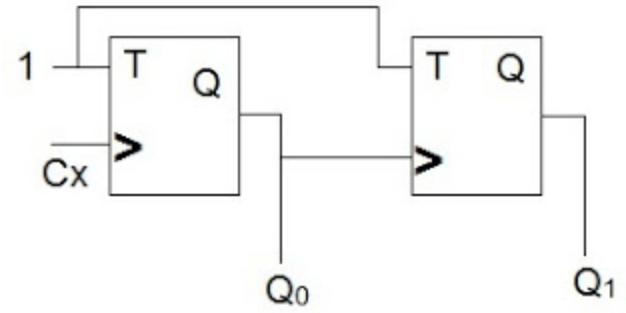
(D) ECL ICs
Answer: B
(UGC net DECEMBER 2008 PAPER II SOLVED No 4)

49. The characteristic equation of D flip-flop is:
(A) Q=1
(B) Q=0
(C) Q=D'
(D) Q=D
Answer: D
(UGCNET-dec2008-ii-14)

50. The characteristic equation of a T flip flop is given by:
(A) $Q_{N+1}=TQ_N$
(B) $Q_{N+1}=T+Q_N$
(C) $Q_{N+1}=T \oplus Q_N$
(D) $Q_{N+1}=T'+Q_N$
Answer: C
(UGCNET-june2009-ii-04)

51. In order to build a MOD-18 counter, the minimum number of flip flops needed is equal to:
(A) 18 (B) 9
(C) 5 (D) 4
Answer: C
(UGC NET Computer Science Solved Paper II DECEMBER 2007 No 8)

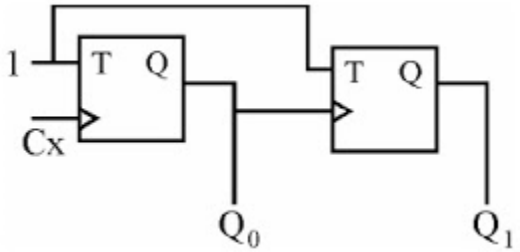
52. What are the final values of Q_1 and Q_0 after 4 clock cycles, if initial values are 00 in the sequential circuit shown below:



(A) 11
(B) 10
(C) 01
(D) 00
Answer: D
(UGCNET-Dec2012-III-23, UGCNET-Dec2013-III-22)

53. Synchronization is achieved by a timing device called a ..... which generates a periodic train of .....
    (A) clock generator, clock pulse
    (B) master generator, clock pulse
    (C) generator, clock
    (D) master clock generator, clock pulse
    Answer: A and D
    (UGCNET-Dec2013-III-51)

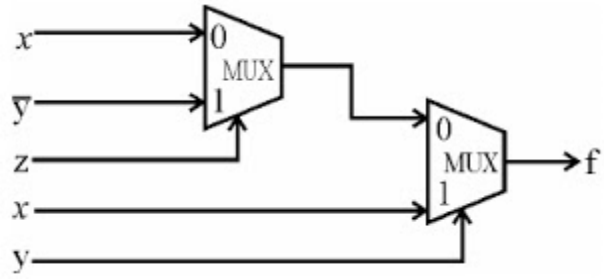
54. What are the final values of Q_1 and Q_0 after 4 clock cycles, if initial values are 00 in the sequential circuit shown below :



    (A) 11
    (B) 10
    (C) 01
    (D) 00
    Answer: D
    (UGCNET-Dec2012-III-23, UGCNET-Dec2013-III-22)

55. 58 lamps are to be connected to a single electric outlet by using an extension board each of which has four outlets. The number of extension boards needed to connect all the light is
    (A) 29
    (B) 28
    (C) 20
    (D) 19
    Answer: D
    (UGCNET-Dec2012-III-29)

56. Consider the below circuit and find the output function f(*x*,y,z).



    (A) *x*z'+*x*y+y'z
    (B) *x*z'+*x*y+y'z'
    (C) *x*z+*x*y+y'z'

(D) *x*z+*x*y'+y'z
Answer: A
(UGCNET-June2012-III-53)

57. A terminal multiplexer has six 1200 bps terminals and 'n' 300 bps terminals connected to it. If the outgoing line is 9600 bps, what is the value of n?
(A) 4
(B) 8
(C) 16
(D) 28
Answer: B
(UGCNET-June2014-III-68)

58. Match the following:
List - I
a. TTL
b. ECL
c. MOS
d. CMOS
List - II
i. High component density
ii. Low power consumption
iii. Evolution of "diode-transistor- logic"
iv. High speed digital circuits
Codes:

	a	b	c	d
(A)	iii	ii	i	iv
(B)	i	iv	iii	ii
(C)	iii	iv	i	ii
(D)	i	ii	iii	iv

Answer: C
(2013 e UGC NET Paper III No 46)

59. The number of flip-flops required to design a modulo-272 counter is:

(A) 8 (B) 9

(C) 27 (D) 11

Answer: B

(UGCNET-June2015-III-6)