Computer Architecture

1. The CPU of a system having 1 MIPS execution rate needs 4 machine cycles on an average for executing an instruction. The fifty percent of the cycles use memory bus. A memory read/write employs one machine cycle. For execution of the programs, the system utilizes 90 percent of the CPU time. For block data transfer, an IO device is attached to the system while CPU executes the background programs continuously. What is the maximum IO data transfer rate if programmed IO data transfer technique is used?

   (A) 500 Kbytes/sec (B) 2.2 Mbytes/sec

   (C) 125 Kbytes/sec (D) 250 Kbytes/sec

   Answer: D

2. A hierarchical memory system that uses cache memory has cache access time of 50 nano seconds, main memory access time of 300 nano seconds, 75% of memory requests are for read, hit ratio of 0.8 for read access and the write-through scheme is used. What will be the average access time of the system both for read and write requests ?

   (A) 157.5 n.sec. (B) 110 n.sec.

   (C) 75 n.sec. (D) 82.5 n.sec.

   Answer: A

   Explanation:

   The average access time of the system for memory read cycle is

   0.8x50+0.2x350=110ns

   The average access time of the system for both read and writes request is

   0.75x110+0.25x300=82.5+75=157.5

3. Suppose a processor does not have any stack pointer registers, which of the following statements is true?

   (A) It cannot have subroutine call instruction.
   (B) It cannot have nested subroutine calls.
   (C) Interrupts are not possible.
   (D) All subroutine calls and interrupts are possible.

   Answer: Marks to All

   Explanation:

   Stack pointer register holds the address of top of stack, which is the location of memory at which the CPU should resume its execution after servicing some interrupt or subroutine call. So if SP register not available then no subroutine call instructions are possible.

4. In an enhancement of a CPU design, the speed of a floating point unit has been increased by 20% and the speed of a fixed point unit has been increased by 10%. What is the overall speed achieved if the ratio of the number of floating point operations to the number of fixed point

operations is 2:3 and the floating point operation used to take twice the time taken by the fixed point operation in original design?

(A) 1.62
(B) 1.55
(C) 1.85
(D) 1.285

Answer: Marks to All

Explanation:

Speed up = Original time taken/ new time taken
Let us say the total number of instruction to be executed is 100
By the ratio 2:3,
Floating point instructions N(Ft) = 40
Fixed point instructions N(Fd) = 60
Before enhancement:
Time taken to process a floating point instruction T(Ft) = 2 units
Time taken to process a fixed point instruction T(Fd) = 1 unit
Total time to execution, T(B) = N(Ft) * T(Ft) + N(Fd) * T(Fd)
= 40×2 + 60×1 = 140 units.
After enhancement:
When speed of floating point processing is increased by 20% means time to execute a floating point instruction is decreased by 20%.
Before T(Ft) was 2 units. Now, time taken to processes a floating point instruction
T(Ft) = 2-2x20% = 1.6 units.
Similarly speed of fixed point processing increased by 10% means time to execute a fixed point instruction is decreased by 10%.
Hence, before T(Fd) was 1 unit. Now time taken to process a fixed point instruction T(Fd) = 1-1x10% = 0.9 units.
Total time to execute T(A) = 40×1.6 + 60x0.9 = 118 units
So, the speed up = T(B)/T(A) = 140/118 = 1.186

5. Let f be the fraction of a computation (in terms of time) that is parallelizable, P the number of processors in the system, and s_p the speed up achievable in comparison with sequential execution – then the s_p can be calculated using the relation :

(A) $\frac{1}{1 - f - f/P}$

(B) $\frac{P}{P - f(P + 1)}$

(C) $\frac{1}{1 - f + f/P}$

(D) $\frac{P}{P + f(P - 1)}$

Answer: C

6. Identify the devices given below with their IC numbers :

(i) USART (a) 8251
(ii) Micro controller (b) 8051
(iii) Interrupt controller (c) 8259
(iv) DMA controller (d) 8257

(i) (ii) (iii) (iv)
(A) (a) (b) (c) (d)
(B) (b) (a) (d) (c)
(C) (c) (d) (a) (b)
(D) (d) (a) (b) (c)
Answer: A

7. The concept of pipelining is most effective in improving performance if the tasks being performed in different stages :

(A) require different amount of time

(B) require about the same amount of time

(C) require different amount of time with time difference between any two tasks being same

(D) require different amount with time difference between any two tasks being different

Answer: B

8. One of the main features that distinguish microprocessor from micro-computers is
(A) words are usually larger in microprocessors.
(B) words are shorter in microprocessors.
(C) microprocessor does not contain I/O devices.
(D) None of the above.

Answer: C

9. A DMA controller transfers 32-bit words to memory using cycle Stealing. The words are assembled from a device that transmits characters at a rate of 4800 characters per second. The CPU is fetching and executing instructions at an average rate of one million instructions per second. By how much will the CPU be slowed down because of the DMA transfer?

(A) 0.06% (B) 0.12%

(C) 1.2% (D) 2.5%

Answer: B

Explanation:

The DMA combines one word from four consecutive characters (bytes) so we get

4800 chars/s = 4800 bytes/s = 1200 words/s (one word = 32 bits = 4 bytes)

If we assume that one CPU instruction is one word wide then

1 million instructions/s = 1 million words/s = 10^6 word/s

So we have 1200 words received during one second and (10^6-1200) words processed by the CPU (while DMA is transferring a word, the CPU cannot fetch the instruction so we have to subtract the number of words transferred by DMA).

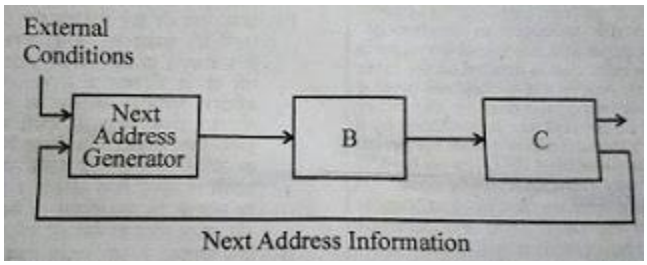
While DMA transfer CPU executes only 10^6 - 1200 = 998800 instructions

[998800 / 10^6] * 100 = 99.88 %

Slowdown = 100 - 99.88 = 0.12%

The CPU will be slowed down by 0.12%.

10. The advantage of ..... is that it can reference memory without paying the price of having a full memory address in the instruction.
    (A) Direct addressing
    (B) Indexed addressing
    (C) Register addressing
    (D) Register Indirect addressing
    Answer: D
11. A byte addressable computer has a memory capacity of 2^m Kbytes and can perform 2^n operations. An instruction involving 3 operands and one operator needs a maximum of
    (A) 3m bits
    (B) m + n bits
    (C) 3m + n bits
    (D) 3m + n + 30 bits
    Answer: D
12. The essential difference between traps and interrupts is
    (A) traps are asynchronous and interrupts are synchronous with the program
    (B) traps are synchronous and interrupts are asynchronous with the program
    (C) traps are synchronous and interrupts are asynchronous with the I/O devices.
    (D) None of these.
    Answer: B
13. Where does a computer add and compare data ?
    (A) Hard disk (B) Floppy disk
    (C) CPU chip (D) Memory chip
    Answer: C
14. Interrupts which are initiated by an instruction are
    (A) Internal (B) External
    (C) Hardware (D) Software
15. The register that stores the bits required to mask the interrupts is .....
    (A) Status register (B) Interrupt service register
    (C) Interrupt mask register (D) Interrupt request register
    Answer: C
16. The general configuration of the microprogrammed control unit is given below:



What are blocks B and C in the diagram respectively?

(1) Block address register and cache memory

(2) Control address register and control memory

(3) Branch register and cache memory

(4) Control address register and random access memory

Answer: 2

17. The three outputs $x_1x_2x_3$ from the 8x3 priority encoder are used to provide a vector address of the form $101x_1x_2x_300$. What is the second highest priority vector address in hexadecimal if the vector addresses are starting from the one with the highest priority?

(A) BC (B) A4

(C) BD (D) AC

Answer: B

18. For the 8-bit word 00111001, the check bits stored with it would be 0111. Suppose when the word is read from memory, the check bits are calculated to be 1101. What is the data word that was read from memory?

(A) 10011001 (B) 00011001

(C) 00111000 (D) 11000110

Answer: B

19. Consider a 32 - bit microprocessor, with a 16 - bit external data bus, driven by an 8 MHz input clock. Assume that the microprocessor has a bus cycle whose minimum duration equals four input clock cycles. What is the maximum data transfer rate for this microprocessor?

(A) $8x10^6$ bytes/sec (B) $4x10^6$ bytes/sec

(C) $16x10^6$ bytes/sec (D) $4x10^9$ bytes/sec

Answer: B

20. Match the following:

List-I

a. Indexed Addressing

b. Direct Addressing

c. Register Addressing

d. Base-Indexed Addressing

List-II

i. is not used when an operand is moved from memory into a register or from a register to memory.

ii. Memory address is computed by adding up two registers plus an (optional) offset.

iii. Addressing memory by giving a register plus a content offset.

iv. can only be used to access global variables whose address is known at compile time.

Codes:

	a	b	c	d
(A)	ii	i	iv	iii
(B)	ii	iv	i	iii
(C)	iii	iv	i	ii
(D)	iii	i	iv	ii

Answer: C

21. A given memory chip has 14 address pins and 8 data pins. It has the following number of locations.
    (A) 28
    (B) 214
    (C) 26
    (D) 212
    Answer: B
22. The number of eight-bit strings beginning with either 111 or 101 is .....
    (A) 64 (B) 128
    (C) 265 (D) None of the above
    Answer: A
23. In which addressing mode, the effective address of the operand is generated by adding a constant value to the contents of register?
    (A) Absolute (B) Indirect
    (C) Immediate (D) Index
    Answer: D
24. The branch logic that provides making capabilities in the control unit is known as
    (A) Controlled transfer (B) Conditional transfer
    (C) Unconditional transfer (D) None of the above
    Answer: A
25. Which of the following logic families is well suited for high-speed operations ?
    (A) TTL (B) ECL
    (C) MOS (D) CMOS
    Answer: B
26. In which addressing mode, the effective address of the operand is generated by adding a constant value to the contents of register?
    (A) absolute mode
    (B) immediate mode
    (C) indirect mode
    (D) index mode
    Answer: D

27. Which one of the following is not an addressing mode?
    (A) Register indirect
    (B) Auto increment
    (C) Relative indexed
    (D) Immediate operand
    Answer: C
28. Computers can have instruction formats with
    (A) only two address and three address instructions
    (B) only one address and two address instructions
    (C) only one address, two address and three address instructions
    (D) zero address, one address, two address and three address instructions
    Answer: D
29. Identify the addressing modes of below instructions and match them :
    (a) ADI (1) Immediate addressing
    (b) STA (2) Direct addressing
    (c) CMA (3) Implied addressing
    (d) SUB (4) Register addressing
    (A) a – 1, b – 2, c – 3, d – 4
    (B) a – 2, b – 1, c – 4, d – 3
    (C) a – 3, b – 2, c – 1, d – 4
    (D) a – 4, b – 3, c – 2, d – 1
    Answer: A
30. Which of the following addressing mode is best suited to access elements of an array of contiguous memory locations?
    (1) Indexed addressing mode
    (2) Base Register addressing mode
    (3) Relative address mode
    (4) Displacement mode
    Answer: 1
31. A micro-instruction format has micro-ops field which is divided into three subfields F1, F2, F3 each having seven distinct micro-operations, condition field CD for four status bits, branch field BR having four options used in conjunction with address field ADF. The address space is of 128 memory locations. The size of micro-instruction is:
    (1) 17 bits
    (2) 20 bits
    (3) 24 bits
    (4) 32 bits
    Answer: 2

50. The speed up of a pipeline processing over an equivalent non-pipeline processing is defined by the ratio:

(A) $S = \frac{n\, t_n}{(k + n - 1)t_p}$

(B) $S = \frac{n\, t_n}{(k + n + 1)t_p}$

(C) $S = \frac{n\, t_n}{(k - n + 1)t_p}$

(D) $S = \frac{(k + n - 1)t_p}{n\, t_n}$

Where n → no. of tasks
t_n → time of completion of each task
k → no. of segments of pipeline
t_p → clock cycle time
S → speed up ratio
Answer: A

50. Which speed up could be achieved according to Amdahl's Law for infinite number of processes if 5% of a program is sequential and the remaining part is ideally parallel?
(1) Infinite
(2) 5
(3) 20
(4) 50
Answer: 3